

High-contrast, highly textured VO₂ thin films integrated on silicon substrates using annealed Al₂O₃ buffer layers

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ABSTRACT

We present vanadium dioxide (VO₂) thin films having high resistivity contrast with silicon substrates through use of crystallized alumina (Al₂O₃) buffer layers, engineered for this purpose. We first optimized the process by depositing VO₂ onto C-plane sapphire substrates prior to alumina thin films. The latter of which were grown via atomic layer deposition on silicon substrates. We then applied rapid thermal annealing (RTA) to crystallize the alumina films. Scanning electron microscopy results indicated a thickness of 107 nm for each VO₂ film, which yielded hot-cold resistivity contrast ratios of 9.76×10^4 , 1.46×10^4 , and 3.66×10^3 , when deposited on the C-plane sapphire, the annealed buffers, and the as-deposited alumina buffers, respectively. Atomic force microscopy of the film surface roughness of the VO₂ films indicated root mean squared roughness (*R_q*) of 4.56 nm, 6.79 nm, and 3.30 nm, respectively, for the films grown on the C-plane sapphire, annealed buffers, and as-deposited buffers. Finally, x-ray diffraction (XRD) of the VO₂ films indicated the desired composition and strong (0h0)/(00h) texturing, when deposited on both the C-plane sapphire and the annealed alumina buffer layers. XRD results indicated a series of peaks corresponding to the α -Al₂O₃/C-plane sapphire, and an XRD analysis of the buffers alone confirmed crystallization of the buffer layer via RTA. The process defined in this paper produced a series of highly textured VO₂ films making them most valuable for the integration of VO₂ with silicon-based devices.

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I. INTRODUCTION

The versatility and quasi-passive attributes of phase change materials (PCMs) in terms of reacting directly or “instinctually” to external stimuli (e.g., heat, pressure, light, and strain) make them particularly useful in sensing and switching applications. Such factors can mean replacing specialized traditional integrated circuits, or improving sensor performance by either exploiting nonlinear behavior, or by creating reconfiguration by activating multiple states of geometry through the strategic actuation of different PCM regions. Vanadium dioxide (VO₂) is particularly appealing for this exploitation/reconfiguration in that it has a low metal-insulator

transition (MIT) temperature (68 °C), which exhibits a reversible, sharp, nonlinear change. These properties are advantageous in terms of lower power and faster switching devices, unlike other PCMs (e.g., germanium-antimony-telluride), that require a high temperature excitation (i.e., ~618 °C) to revert to a dielectric state.¹ Although the temperature and hysteresis width of the VO₂ phase transition is tunable, as is the MIT itself on a domain level,² this work focuses on growing VO₂ films using silicon (Si) substrates that exhibit similar properties to that grown on a C-plane sapphire.

The C-plane sapphire was chosen because it yields VO₂ films whose electrical properties closely resemble those of bulk VO₂:

particularly, a transition temperature of 68 °C.³ Other works have presented comparisons of high-quality VO₂ films on C-plane with R-^{3,4} and M-plane⁴ sapphire, but both alternate sapphire substrates show a shift in transition temperature. All experimental VO₂ films in this work maintain the transition temperature of 68 °C so the most direct control comparison is the C-plane sapphire.

VO₂ applications include radio frequency (RF) switches,^{5,6} infrared asymmetric transmission limiters,⁷ and thermal imaging sensors.⁸ Its sharp change in resistivity makes it an ideal material for a shunt RF switch, where the room temperature VO₂ is RF-transparent in the passing state and heated to a conducting state to short the signal line to the ground plane, causing high reflection.^{6,9} Such switches and similar mechanisms are useful in a multitude of RF applications, including millimeter wave phase shifters¹⁰ and reactive power limiters,⁶ reconfigurable antennas,¹¹ and metasurfaces.¹² As Si is widely used in a multitude of such research and industry concepts, additional applications of VO₂ such as micro-actuators,^{2,13,14} thermochromics,^{2,15,16} optical modulators,^{2,17} field-effect transistors,¹⁸ power meters,² electrostatic discharge protection,¹⁹ and gas sensors² give merit to the integration of VO₂ on Si substrates. The key novelty of this work is the deposition of high-contrast VO₂ films on Si substrates through use of annealed Al₂O₃ buffer layers, thus paving the way for the easy integration of such devices in the future.

Unfortunately, the limited deposition of state of the art VO₂ thin films to single crystal sapphire substrates,⁴ where there is a strong lattice match between the C-plane sapphire and VO₂, currently hinders the pragmatic use of VO₂. Specifically, the extremely low etch rates²⁰ and lack of semiconductor properties prevent the use of sapphire for bulk etch/micromachining and in standard device processes. Indeed, silicon substrates are most commonly used in device processing, for both traditional integrated circuit applications and techniques used in micro-electromechanical systems. Unfortunately, the large lattice mismatch between Si and VO₂ inhibits the efficacy of direct deposition of VO₂. Such films exhibit comparatively small change in the resistivity ($<1 \times 10^3$) and large hysteresis (~ 8 °C) in the phase transition region.²¹ In cases where larger hysteresis is beneficial, like memory applications, a recent overview discusses intentional manipulation of hysteresis.² Intuitively, it is better to start with VO₂ having bulk properties and modify from there than to accept a VO₂ film with weak orientation and low phase purity. In Table I, we provide a comparison of theoretical lattice mismatch of VO₂ on both the C-plane sapphire and Si.

To improve the performance of VO₂ thin films on Si substrates, several materials for buffer layers such as yttria-stabilized zirconia,²² HfO₂,²³ and amorphous Al₂O₃^{21,24} were proposed. The advantage of this work over previous studies using Al₂O₃ buffer layers is the new comparison of VO₂ on amorphous alumina with VO₂ on annealed, polycrystalline alumina buffers. Another

distinguishing factor is that this work also uses DC sputtering rather than RF sputtering²¹ and yields a higher resistivity contrast ratio.^{21,24} Although thermally oxidized silicon dioxide buffer layers²⁵ have shown resistivity contrast ratios of 1.3×10^4 , this fabrication technique is limited to Si and cannot be adapted to other substrates. It is, however, possible to use the thin film atomic layer deposition (ALD) technique with various substrates such as GaAs or GaN.^{26,27}

VO₂ films deposited on single crystal sapphire substrates have been described as epitaxial, since their sapphire lattice determines their orientation.^{28–30} The VO₂ films presented in this work have clear epitaxial relation to their underlying sapphire substrates and annealed buffers, but we refrain from using the term *epitaxial* for two reasons; the sputtering process described here is not a standard epitaxy process, and in the buffer layer case, the underlying growth surface is polycrystalline, not monocrystalline. However, we also abstain from using the term *polycrystalline* to describe the VO₂, as it discounts the substantial dependence of our VO₂ preferred texturing on the underlying crystal substrate and buffer layer structures. Therefore, we use the modified term *textured-epitaxial* to convey the dependence of the VO₂ films' structure on epitaxial interactions with both the single crystal sapphire and local sites in the polycrystalline alumina buffer. As such, we sought to create a polycrystalline α -Al₂O₃ buffer layer to create similar VO₂ growth conditions on the bulk sapphire. The alumina buffer is not categorized as, nor intended to be epitaxial nor textured-epitaxial in itself, but rather it is intended to eliminate the effect of the Si diamond cubic lattice on the VO₂. The VO₂, Si, and Al₂O₃ lattices are illustrated conceptually as cross sections in Fig. 1.

Our proposed solution is to implement alumina buffer layers deposited using ALD, which we crystallize using rapid thermal annealing (RTA). X-ray diffraction (XRD) illustrates no crystallographic differences of the VO₂ structure when deposited on annealed polycrystalline alumina buffer vs C-plane sapphire, whereas VO₂ deposited on amorphous alumina buffer indicates significantly reduced crystallinity. Furthermore, XRD analysis of alumina thin films deposited on diamond silicon without VO₂ confirms the emergence of polycrystallinity upon annealing. The VO₂ films used here were deposited with DC reactive sputtering, which is advantageous over a number of techniques such as pulsed laser deposition, solgel, ALD, chemical vapor deposition, molecular beam epitaxy,¹⁶ metal organic chemical vapor deposition,³⁰ and hydrothermal growth³¹ making it possible to extend the sputtering to a larger batch processing for efficient manufacturing.

II. MATERIALS AND METHODS

A. Thin film deposition

1. Vanadium dioxide deposition

This VO₂ deposition process is an extension of previous efforts to create reconfigurable terahertz filters with VO₂ using reactive sputtering.³² An incrementing of the O₂ flow during annealing and controlling for a variation in the deposition rate between trials increased the resistivity contrast ratio from 7×10^4 to 9.76×10^4 and decreased the hysteresis width from 6 °C to 4 °C. As the measurement process was also improved, the 6 °C hysteresis

TABLE I. Lattice mismatch of tetragonal rutile VO₂ as deposited on a C-plane sapphire and (100) silicon.

	C-plane sapphire (α -Al ₂ O ₃)	Silicon-d ($Fd\bar{3}m$)
VO ₂ ($P4_2/mnm$)	4.19%	16.1%

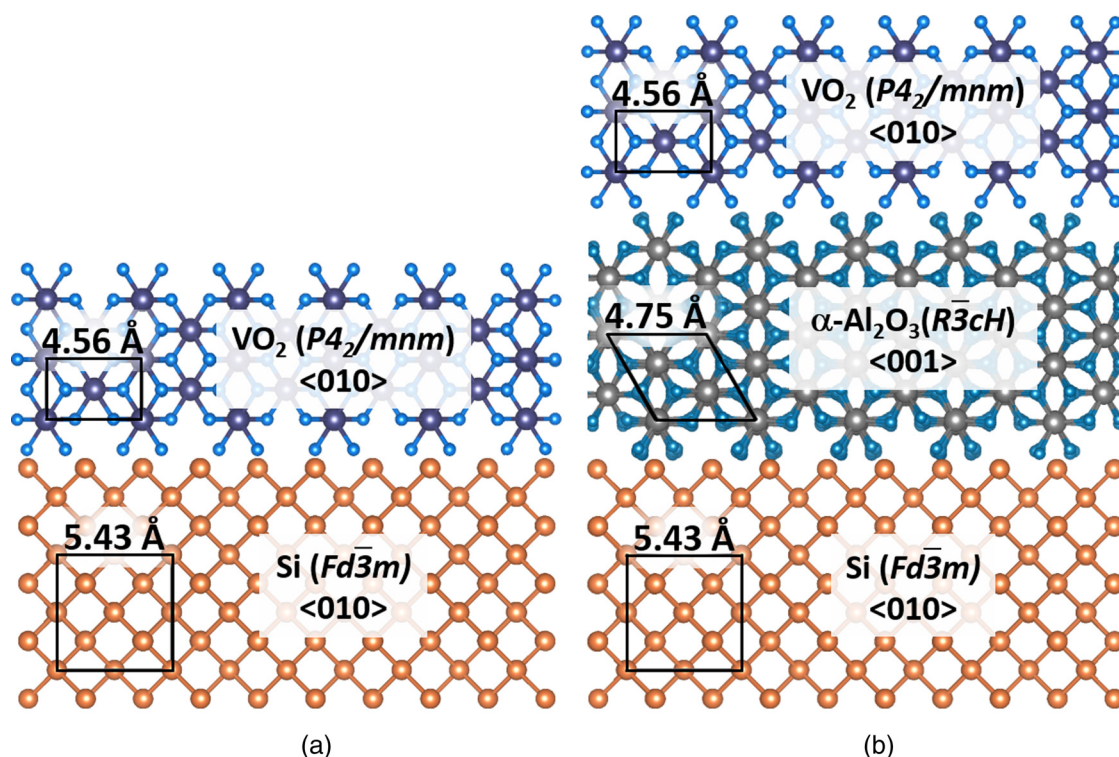


FIG. 1. (a) Crystallographic schematic of rutile VO₂ on diamond silicon illustrating the large lattice parameter mismatch that leads to high strain vs (b) rutile VO₂ on an alumina buffer layer on silicon eases the lattice parameter mismatch lowering the overall strain and increasing the electrical resistivity contrast.

figure refers to early trials within this work. The C-plane sapphire wafers are cleaned with organic solvents and dried. A dummy Si wafer is then used to eliminate contaminants in the sputtering chamber and coat the chamber in VO₂ prior to deposition on the experimental sample.

First, the sample is cleaned with plasma for 7 min using 20 sccm Ar⁺ plasma and 50 W RF power at 4.0 Pa. Next, the chamber is heated at vacuum to 650 °C prior to flowing 1.62 sccm O₂ and 20 sccm Ar (7.5% O₂; total gas ratio) at 1.33 Pa pressure. The DC power is increased to 250 W and the sputtering target shutter left open for the time required to ensure the deposition of 107 nm of VO₂, based upon the rate measured. Once the deposition is complete, the sample is annealed, *in situ*, at the same temperature in 1.33 Pa, 10 sccm O₂ environment for 15 min. We use an experimental process, the iterative results of which are detailed in Sec. III A, to establish these parameters. Overall, we established them through five key iterations, described in Table II in Sec. III A.

We discovered that the deposition rate can vary significantly between trials when the same process was employed multiple times with varying results. However, controlling for the variable deposition rate (by measuring before each deposition) returned the expected results, thus confirming repeatability of this process. Therefore, the final iteration of the process is also used to deposit on the experimental buffer layers as well.

2. Alumina deposition and annealing

To fabricate the alumina thin films, Al₂O₃ with a thickness of 45 nm is deposited onto the Si substrates. The precursors are trimethylaluminum and H₂O heated to 300 °C with N₂ as the purging gas, followed by the RTA process at 950 °C for 60 s in N₂ ambient. This process is essential for the deposition of high-contrast, highly textured VO₂ films since the crystallization of alumina creates a stronger basis for VO₂ growth than do the amorphous films.

B. Characterization methods

Electrical resistivity, crystallinity, thickness, and surface morphology serve as the criteria for characterizing the VO₂ films grown in this study. To capture the full heating and cooling hysteresis loop for each sample, the resistivity was measured using a 4-point probe, hot plate, and surface probe thermometer. Parallel-beam x-ray diffraction (XRD) is next used to determine the crystal structure of the VO₂ and for the Al₂O₃ buffers. All XRD patterns are collected on a Rigaku SmartLab diffractometer with Cu-Kα radiation, in a 2θ/θ collection mode, with a step size of 0.01°, a speed of 12 s/step, and all slits set to 1.00 mm. Scanning electron microscopy (SEM) is used to measure thickness and observe crystal grain structure and surface morphology, and atomic force microscopy (AFM) used to measure the surface roughness.

TABLE II. VO₂ deposition trials. Rather than listing the constant process variables in the table, they are described in the text for clarity. Trials deemed that process failures are also omitted and key process changes marked with *.

Sample ID	Ar flow (sccm)	O ₂ flow (sccm)	O ₂ :total gas ratio (%)	Deposition time (min:s)	Annealing O ₂ flow (sccm)	Resistivity contrast ratio (unitless)	Hysteresis width (°C)	Transition range (°C)
A	19.96	1.58	7.34	16:40	1.58	3.11×10^4	6	12
B	19.96	*1.62	*7.51	16:40	*1.62	1.99×10^4	6	18
C	19.96	*1.58	*7.34	16:40	*4.96	6.29×10^4	6	12
D	19.96	1.58	7.34	16:40	*9.97	6.88×10^4	4	12
E	19.96	1.58	7.34	*20:00	9.97	9.76×10^4	4	12

III. RESULTS AND DISCUSSION

A. Temperature-dependent resistivity

Resistivity contrast ratio, defined as the resistivity at room temperature divided by that above the MIT, is a key figure of merit for VO₂ thin films. A hot plate, surface probe thermometer, and 4-point probe were used to measure the sheet resistance over the phase change of the VO₂ samples. We measured the samples from room temperature through and past the transition region and again during the cool down to capture the full hysteretic loop of the phase change behavior. We then multiplied the sheet resistance values by the thickness to calculate resistivity.

As indicated in the resistivity hysteresis loops in Fig. 2, on the C-plane sapphire, our films exhibit state of the art performance, with nearly five orders of magnitude resistivity contrast ratio at 9.76×10^4 . The iterations of the fabrication process are detailed in Table II with their respective contrast ratio and hysteresis width results. A significantly decreased resistivity contrast ratio at 3.66×10^3 , characterized the VO₂ thin films deposited on as-deposited alumina buffer layers. Such findings are expected in that ALD alone yields amorphous films that cannot create a lattice match for VO₂ growth. Based upon our hypothesis that RTA is suitable in transforming the alumina buffer layer from amorphous to polycrystalline, we deposited VO₂ on these annealed buffer layers. The result was an increase in the resistivity contrast ratio by a factor of 4, which yielded a new ratio of 1.46×10^4 .

B. X-ray diffraction

Parallel-beam XRD analysis confirmed that depositing VO₂ on annealed polycrystalline alumina does not cause a change in the crystal structure compared to when it is deposited on the C-plane sapphire, with both yielding monoclinic (*P2₁/c*) VO₂ at room temperature. Figure 3 illustrates low-crystallinity monoclinic VO₂ when deposited on amorphous alumina with a low intensity (020)/(002) peak around 39.8°. However, when deposited on annealed polycrystalline alumina and C-plane sapphire, there are strong, clear diffraction peaks at 39.8°, corresponding to VO₂ texturing in the (020) or (002) planes supported by the peaks at approximately 86°, corresponding to the (040) or (004) plane. Because the d-spacings of the (002), and (020) peaks as well as the (004), and (040) peaks

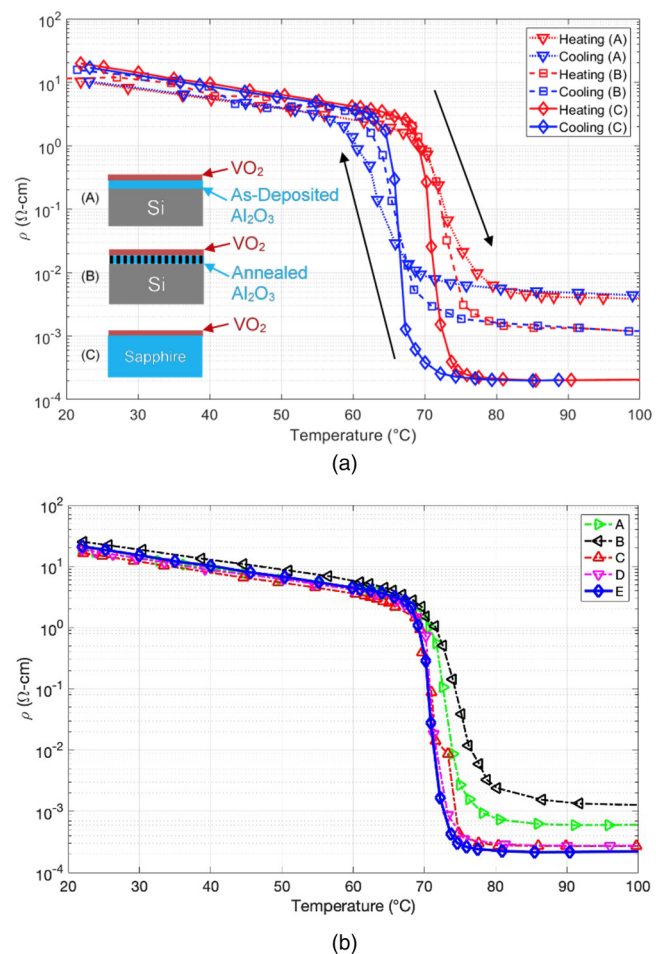


FIG. 2. Resistivity vs temperature measurements comparing (a) the electrical performance of the VO₂ thin films on ALD thin films, both amorphous (as-deposited) and annealed, as well as bulk crystalline C-plane sapphire wafers and (b) each deposition trial iteration as detailed in Table I. Sample IDs are labeled A through E, corresponding to the process details in Table I. Sample A is the first trial, and Sample E is from the finalized process.

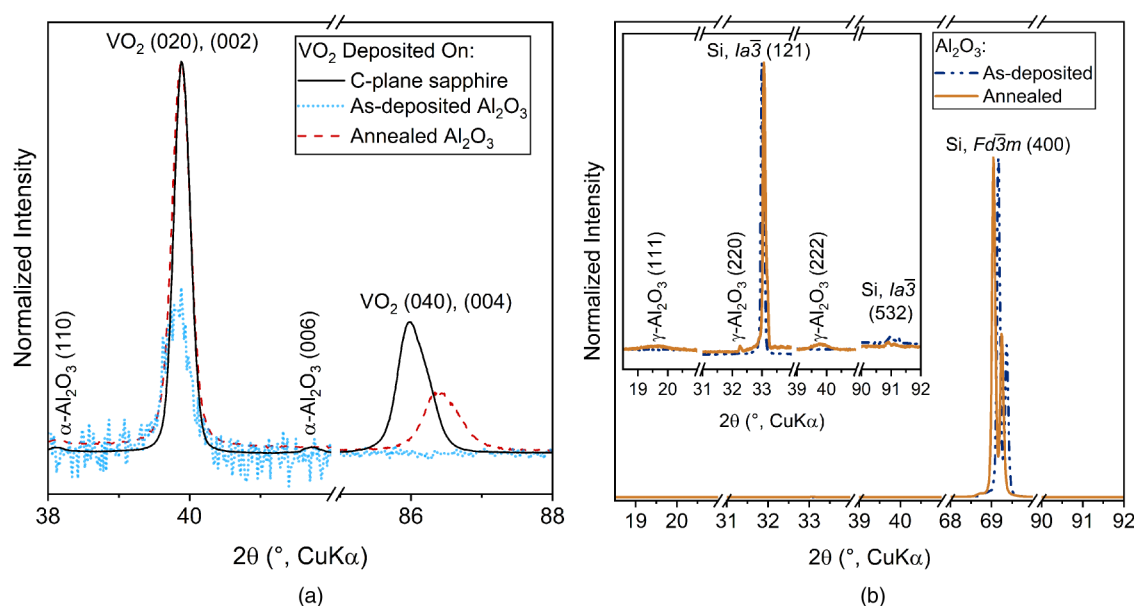


FIG. 3. XRD of (a) monoclinic VO₂ deposited on a C-plane sapphire, 45 nm annealed alumina, and 45 nm as-deposited alumina, illustrating higher crystallinity VO₂ and (020)/(002) texture when deposited on the annealed alumina (b) 25 nm alumina before and after annealing illustrating polycrystallinity emerging on top of the diamond silicon substrate with a silicon intermediate, *Ia* $\bar{3}$.

are almost exactly coincidental, they cannot be differentiated in this circumstance.^{3,33–41} These 2θ ranges were chosen because no other diffraction peaks were shown during previous XRD scans on similar samples, which can be found in figures in the [supplementary material](#). Other literature corroborates these two peaks and shows that for (020)/(002) textured VO₂, the rest of the spectrum does not show any peaks of interest.^{3,4}

VO₂ on the C-plane sapphire has a slight (040)/(004) peak shift of 0.5° toward a higher 2θ from simulated bulk diffraction patterns; whereas, VO₂ on the annealed polycrystalline alumina (040)/(004) peak shift of 0.9° toward a higher 2θ angle. However, both (040)/(004) peaks are broadened. This shift is most likely due to the highly non-uniform but overall compressive strain on the system, which is also supported by the (040)/(004) peak broadening. The peak broadening depends on the Bragg angle, indicating that it is most likely due to a combination of the increase in strain, which could be different in individual grains, and crystallite size. This broadening originates from the lattice mismatch between the Si-d substrate (*Fd* $\bar{3}m$) and the α -Al₂O₃ buffer (*R* $\bar{3}cH$), shown in [Fig. 3](#), which strains the buffer placing extra strain on the VO₂ that is absent when deposited on the single-crystalline C-plane sapphire. Additionally, there is strain inherent in the VO₂ films; since they are deposited above the MIT, they are grown in the tetragonal rutile structure and subsequently transition to monoclinic when cooled. [Figure 3](#) illustrates the initial crystallization of VO₂ with this preferred (020) growth texture even without the alumina anneal. However, the low signal-to-noise ratio and absence of the (040) peak indicates the presence of very little crystalline VO₂ without annealing the buffer.

The small peaks at 38.1° in both the C-plane sapphire and annealed alumina and at 41.7° in the C-plane sapphire correspond to the (110) and (006) planes, respectively, in the α -Al₂O₃ substrate and buffer. However, when Al₂O₃ is deposited and annealed on the silicon substrate by itself, it crystallizes into γ -Al₂O₃ (*Fd* $\bar{3}m$) as shown in [Fig. 2\(b\)](#). The 19.6°, 32.3°, and 39.3° correspond to the (111), (220), and (222) planes in γ -Al₂O₃, respectively. As with VO₂ deposition, there are slight peak shifts of 0.2° and 0.4° for the (211) and (220) peaks as compared to simulated bulk diffraction patterns associated with the lattice mismatch placing strain on the system. Since the RTA performed on the alumina buffer creates only γ -Al₂O₃, it is likely that some local topotaxial conversion^{28,42} in the alumina occurs during the VO₂ deposition process from the γ -phase to α -phase.

In the XRD scans of alumina buffers on Si, the highest intensity peak coincides with the (100) single-crystalline Si-d (*Fd* $\bar{3}m$) substrate. However, the second highest intensity peak at the 33.2° corresponds to the (121) plane of Si-HP (*Ia* $\bar{3}$), which is supported by the presence of two peaks at approximately 91° indexing to the (532) plane of Si-HP. The presence of this phase most likely manifests as a lattice transition layer between the Si-d substrate and the crystallized γ -Al₂O₃ due to a large lattice mismatch of 46.2%. Similar to the VO₂ crystallized on annealed Al₂O₃, the slight peak shifts in the XRD patterns are due to the strain, with peak broadening due to a combination of larger crystallite size and the non-uniformity of the strain from individual grains in the annealed polycrystalline buffer.

In [Fig. 4](#), we show the theoretical lattice mismatch values of the deposited materials with the substrates and buffers. The low lattice mismatch of the tetragonal rutile VO₂ (R), which is

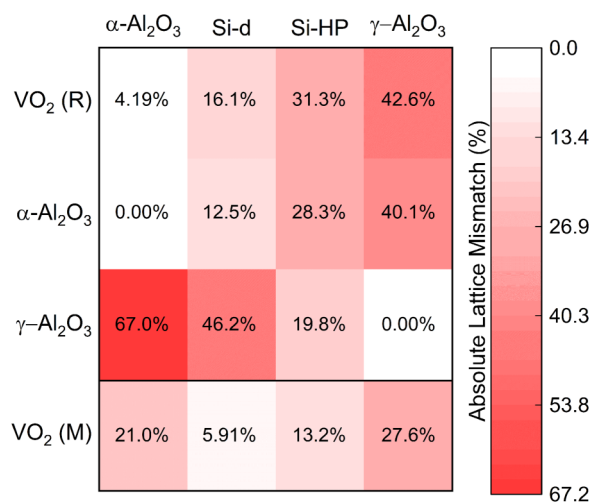


FIG. 4. Absolute lattice mismatch of the deposited compounds (left) on the substrates or buffers (top). VO_2 (M) is included, since that is the phase observed in XRD. However, it is not the growth lattice, and therefore its mismatch is not necessarily considered.

associated with the deposition temperature, is the central consideration for forming highly textured VO_2 . We perform the deposition process at 650°C , which is well above the MIT, to ensure the creation of a VO_2 (R) film during the growth and annealing process. This VO_2 (R) film evolves into VO_2 (M) upon cooling. From these observations, we conclude that the annealed alumina ultimately mimics to a significant degree the growth conditions leading to a highly crystalline VO_2 (M), which the C-plane sapphire provides.

With the similarities in mind between VO_2 as deposited on the C-plane sapphire and annealed alumina, we classify the latter as textured-epitaxial as well. The polycrystalline nature of the buffer and the sputtering/*in situ* annealing process preclude using the term epitaxial, but the data strongly suggest *local* epitaxial interactions as the cause of the similarity in these films.

C. Scanning electron microscopy

Each VO_2 film is 107 nm thick, with negligible variation based on the crystallinity of the buffer layer. To confirm the thickness of the films, we observed a cross section of each sample deposited on an alumina buffer layer using SEM. As shown in Fig. 5, the grains of the VO_2 thin films are evident in both the samples with annealed and as-deposited buffer layers, with the film thickness not

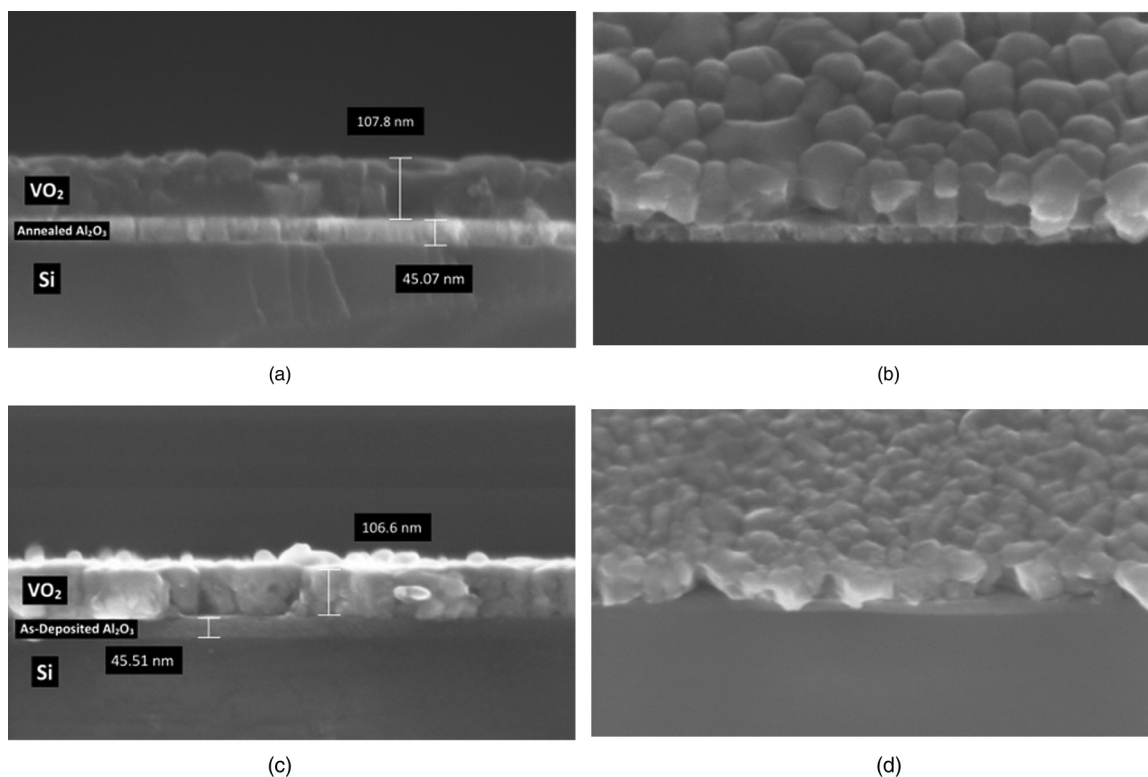


FIG. 5. SEM micrographs of VO_2 deposited on [(a) and (b)] annealed Al_2O_3 and [(c) and (d)] as-deposited Al_2O_3 buffer layers. Each buffer layer is 45 nm thick, and each VO_2 film is 107 nm thick. The left column [(a) and (c)] shows cross sections of the films, and the right column [(b) and (d)] shows the same samples on a 45° tilt.

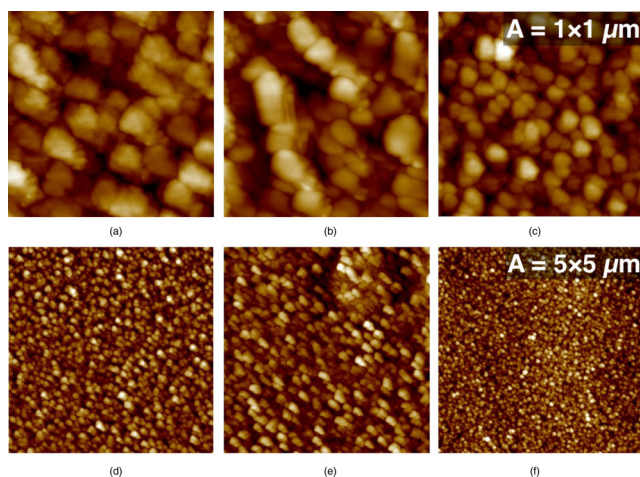


FIG. 6. AFM images of $1 \times 1 \mu\text{m}$ (top row) and $5 \times 5 \mu\text{m}$ (bottom row) of VO_2 on the C-plane sapphire [(a) and (d)]; the annealed alumina buffer [(b) and (e)]; and the as-deposited alumina [(c) and (f)].

dependent on the buffer layer properties. Note also the crystallization of the buffer layer as hypothesized and observed using XRD by the visual inspection of the micrographs compared in Fig. 5. This observation of the crystal formation further corroborates the hypothesis that the application of RTA to ALD alumina thin films creates a basis for higher contrast, more highly textured VO_2 than as-deposited alumina.

D. Atomic force microscopy

Additionally, we performed AFM to study the VO_2 films' surface roughness. The VO_2 grown on as-deposited alumina showed the lowest root mean squared roughness (R_q), of 3.30 nm, the results of which were expected as it was the most amorphous film as shown by XRD and SEM. The R_q roughness of the VO_2 on annealed alumina and C-plane sapphire were 6.79 nm and 4.56 nm, respectively. Although VO_2 on the C-plane sapphire exhibits a more predominant crystalline arrangement, as shown by XRD, it was smoother, as indicated by the difference in roughness between the sapphire wafer and the annealed alumina buffer. Sapphire is polished to an arithmetic mean (R_a) roughness of <0.3 nm according to the manufacturer, while the R_a roughness of the annealed alumina thin film is 0.68 nm, measured using AFM. Note also in Fig. 6 that VO_2 on as-deposited alumina has a rounded grain structure and the smallest size, while VO_2 on annealed alumina has larger grains with some variance in size and shape, and VO_2 on the C-plane sapphire has consistently sized and shaped grains.

IV. CONCLUSIONS

We developed a repeatable process for depositing high-resistivity contrast, textured-epitaxial VO_2 on C-plane sapphire and on alumina thin film buffer layers on silicon substrates, using DC sputtering. The textured-epitaxial VO_2 on sapphire exhibited state of the art resistivity contrast of 9.76×10^4 , the polycrystalline VO_2

on as-deposited alumina showed resistivity contrast of 3.66×10^3 , and annealing the alumina increased that result by a factor of 4 to 1.46×10^4 in the respective textured-epitaxial VO_2 . XRD, SEM, and AFM analysis of our films shows that the annealed alumina buffer layers produce textured-epitaxial VO_2 films similar to those grown directly on the bulk C-plane sapphire, as well as crystallization of the alumina, particularly in the γ -phase. Our VO_2 deposition process, combined with silicon substrates, creates high-contrast, textured-epitaxial films; thus, it is more easily integrated with a much wider range of devices than VO_2 strictly grown on sapphire wafers.

SUPPLEMENTARY MATERIAL

See the [supplementary material](#) for a full 2θ angle range (10° – 70°) x-ray diffraction scan of VO_2 on a C-plane sapphire substrate.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The data that support the findings of this study are available within the article and its [supplementary material](#).

REFERENCES

- 1A. Sarangan, J. Duran, V. Vasilyev, N. Limberopoulos, I. Vitebskiy, and I. Anisimov, *IEEE Photonics J.* **10**, 2200409 (2018).
- 2R. Shi, N. Shen, J. Wang, W. Wang, A. Amini, N. Wang, and C. Cheng, *Appl. Phys. Rev.* **6**, 011312 (2019).
- 3T.-H. Yang, R. Aggarwal, A. Gupta, H. Zhou, R. J. Narayan, and J. Narayan, *J. Appl. Phys.* **107**, 053514 (2010).
- 4Y. Zhao, J. Hwan Lee, Y. Zhu, M. Nazari, C. Chen, H. Wang, A. Bernussi, M. Holtz, and Z. Fan, *J. Appl. Phys.* **111**, 053533 (2012).
- 5F. Dumas-Bouchiat, C. Champeaux, A. Catherinot, A. Crunteanu, and P. Blondy, *Appl. Phys. Lett.* **91**, 223505 (2007).
- 6A. Crunteanu, J. Givernaud, J. Leroy, D. Mardivirin, C. Champeaux, J.-C. Orlianges, A. Catherinot, and P. Blondy, *Sci. Technol. Adv. Mater.* **11**, 065002 (2010).
- 7R. Thomas, E. Makri, T. Kottos, B. Shapiro, and I. Vitebskiy, *Phys. Rev. A* **98**, 053806 (2018).
- 8C. Chen, X. Yi, X. Zhao, and B. Xiong, *Sens. Actuators A* **90**, 212 (2001).
- 9J. Lee, D. Lee, S. J. Cho, J.-H. Seo, D. Liu, C.-B. Eom, and Z. Ma, *Appl. Phys. Lett.* **111**, 063110 (2017).
- 10C. Hillman, P. A. Stupar, J. B. Hacker, Z. Griffith, M. Field, and M. Rodwell, in IEEE MTT-S International Microwave Symposium Digest, Tampa, FL (2014).
- 11D. Anagnostou, D. Torres, T. Teeslink, and N. Sepulveda, *IEEE Antennas Propag. Mag.* (published online 2020).
- 12M. R. M. Hashemi, S.-H. Yang, T. Wang, N. Sepulveda, and M. Jarrahi, *Sci. Rep.* **6**, 35439 (2016).

- ¹³R. Cabrera, E. Merced, and N. Sepulveda, *J. Microelectromech. Syst.* **23**, 243 (2014).
- ¹⁴E. Merced, N. Dávila, D. Torres, R. Cabrera, F. E. Fernández, and N. Sepúlveda, *Smart Mater. Struct.* **21**, 105009 (2012).
- ¹⁵Y. Choi, Y. Jung, and H. Kim, *Thin Solid Films* **615**, 437 (2016).
- ¹⁶H.-C. Ho, Y.-C. Lai, K. Chen, T. D. Dao, C.-H. Hsueh, and T. Nagao, *Appl. Surf. Sci.* **495**, 143436 (2019).
- ¹⁷L. Sánchez, S. Lechago, and P. Sanchis, *Opt. Lett.* **40**, 1452 (2015).
- ¹⁸K. Abbas, J. Hwang, G. Bae, H. Choi, and D. J. Kang, *ACS Appl. Mater. Interfaces* **9**, 13571 (2017).
- ¹⁹S. M. Bohaichuk, M. M. Pelella, Y. Sun, Z. Zhang, S. Ramanathan, and E. Pop, *IEEE Electron Device Lett.* **41**, 292 (2020).
- ²⁰K. R. Williams, K. Gupta, and M. Wasilik, *J. Microelectromech. Syst.* **12**, 761 (2003).
- ²¹Y. Xiong, Q.-Y. Wen, Z. Chen, W. Tian, T.-L. Wen, Y.-L. Jing, Q.-H. Yang, and H.-W. Zhang, *J. Phys. D Appl. Phys.* **47**, 455304 (2014).
- ²²A. Gupta, R. Aggarwal, P. Gupta, T. Dutta, R. J. Narayan, and J. Narayan, *Appl. Phys. Lett.* **95**, 111915 (2009).
- ²³B. Viswanath, C. Ko, Z. Yang, and S. Ramanathan, *J. Appl. Phys.* **109**, 063512 (2011).
- ²⁴D. Zhang, T. Wen, Y. Xiong, D. Qiu, and Q. Wen, *Nano Micro Lett.* **9**, 29 (2017).
- ²⁵S. J. Yun, J. W. Lim, J.-S. Noh, B.-G. Chae, and H.-T. Kim, *Jpn. J. Appl. Phys.* **47**, 3067 (2008).
- ²⁶S. Jiang, G. He, M. Liu, L. Zhu, S. Liang, W. Li, Z. Sun, and M. Tian, *Adv. Electr. Mater.* **4**, 1700543 (2018).
- ²⁷A. Hiraiwa, T. Sasaki, S. Okubo, K. Horikawa, and H. Kwarada, *J. Appl. Phys.* **123**, 155303 (2018).
- ²⁸A. Matsuda, Y. Nozawa, S. Kaneko, and M. Yoshimoto, *Appl. Surf. Sci.* **480**, 956 (2019).
- ²⁹K. Okimura and Y. Suzuki, *Jpn. J. Appl. Phys.* **50**, 065803 (2011).
- ³⁰A. M. Makarevich, I. I. Sadykov, D. I. Sharovarov, V. A. Amelichev, A. A. Adamenkov, D. M. Tsymbarenko, A. V. Plokhii, M. N. Esaulkov, P. M. Solyankin, and A. R. Kaul, *J. Mater. Chem. C* **3**, 9197 (2015).
- ³¹R. Wang, H. Wang, Z. An, J. He, C. Zhang, G. Pan, and X. Li, *J. Appl. Phys.* **125**, 163104 (2019).
- ³²V. Sanphuang, N. Ghalichechian, N. K. Nahar, and J. L. Volakis, *IEEE Trans. Terahertz Sci. Technol.* **6**, 583 (2016).
- ³³A. Gupta, J. Narayan, and T. Dutta, *Appl. Phys. Lett.* **97**, 151912 (2010).
- ³⁴J. Nag, E. A. Payzant, K. L. More, and R. F. Haglund, *Appl. Phys. Lett.* **98**, 251916 (2011).
- ³⁵J. Narayan and V. M. Bhosle, *J. Appl. Phys.* **100**, 103524 (2006).
- ³⁶Y. Zhou and S. Ramanathan, *J. Appl. Phys.* **112**, 074114 (2012).
- ³⁷L. L. Fan, Y. F. Wu, C. Si, C. W. Zou, Z. M. Qi, L. B. Li, G. Q. Pan, and Z. Y. Wu, *Thin Solid Films* **520**, 6124 (2012).
- ³⁸L. L. Fan, Y. F. Wu, C. Si, G. Q. Pan, C. W. Zou, and Z. Y. Wu, *Appl. Phys. Lett.* **102**, 011604 (2013).
- ³⁹Y. X. Guo, Y. F. Liu, C. W. Zou, Z. M. Qi, Y. Y. Wang, Y. Q. Xu, X. L. Wang, F. Zhang, and R. Zhou, *Appl. Phys. A* **115**, 1245 (2014).
- ⁴⁰P. Mandal, A. Speck, C. Ko, and S. Ramanathan, *Opt. Lett.* **36**, 1927 (2011).
- ⁴¹Z. P. Wu, S. Yamamoto, A. Miyashita, Z. J. Zhang, K. Narum, and H. Naramoto, *J. Phys. Condens. Matter* **10**, L765 (1998).
- ⁴²R. D. Shannon and R. C. Rossi, "The Definition of Topotaxy," eScholarship, Lawrence Berkeley National Laboratory, Recent Work (1963).